

Abstract

A processor includes scheduling circuitry and an associated interval computation element. The scheduling circuitry schedules data blocks for transmission from a plurality of transmission elements, and is configured for utilization of at least one time slot table in scheduling the data blocks for transmission. The interval computation element, which may be implemented as a script processor, is operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table. The transmission interval is adjustable under control of the interval computation element so as to facilitate the maintenance of a desired service level for one or more of the transmission elements. The interval computation element operates under software control in at least one of determining and adjusting the transmission interval, and may be operative to determine periodically if the transmission interval requires adjustment in order to maintain the desired service level for one or more of the transmission elements.